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09/668,407	09/22/2000	Tam-Anh Chu	84834-US2	2364
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STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			MOORE JR, MICHAEL J	
			ART UNIT	PAPER NUMBER
			2616	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/668,407

Applicant(s)

CHU, TAM-ANH

Examiner

Michael J. Moore, Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11, 17-27 and 33-43 is/are rejected.
- 7) ☒ Claim(s) 12-16, 28-32 and 44-48 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments in the Appeal Brief filed 6/7/06, with respect to the rejection(s) of claim(s) **1-11, 17-27, and 33-43** have been fully considered and are persuasive. Therefore, these rejections have been withdrawn. Accordingly, the finality of the previous Office Action has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as provided below.

### ***Claim Objections***

2. Claims **1 and 33** are objected to because of the following informalities:

Regarding claim **1**, on line 7, an objection is made to the use of the phrase "may be" as this phrase constitutes optional language that does not further limit this claim. See MPEP 2106, II, C. A suggestion would be to replace the phrase "may be" with "is".

Regarding claim **33**, on line 13, an objection is made to the use of the phrase "may be" as this phrase constitutes optional language that does not further limit this claim. See MPEP 2106, II, C. A suggestion would be to replace the phrase "may be" with "is".

Also, on line 13, an objection is made to the phrase "the buffer memory". It is unclear whether this limitation is referring to the "input buffer memory", the "output buffer memory" or both of these memories.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43** are rejected under 35 U.S.C. 102(e) as being anticipated by Sang et al. (U.S. 6,401,147) (hereinafter "Sang"). *Sang* teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding claim **1**, "a buffer memory of a first type to store data associated with a connection identifier corresponding to a channel in a network" is anticipated by the receive FIFO buffer (buffer memory of first type) of MAC unit 20 of Figure 2 that stores data packets having header information (connection identifier) received from network stations 14 (connection) of Figure 1 as spoken of on column 6, lines 47-61.

"The data being organized into at least one chunk based on a linked list" is anticipated by the data packets received by a corresponding MAC port and stored in a corresponding received FIFO (organized into at least one chunk).

"The connection identifier identifying a connection in the channel" is anticipated by the packet header information (connection identifier) that includes source, destination, and VLAN address information as spoken of on column 6, lines 58-61.

"The data being part of a data stream associated with the connection" is anticipated by the data packets received by MAC unit 20 of Figure 2 that are associated with a network station 14 of Figure 1.

Lastly, "a packet memory of a second type coupled to the buffer memory to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory" is anticipated by external SSRAM memory block 36 (packet memory of second type) coupled to MAC unit 20 of Figure 1 that receives burst writes of data from a corresponding receive FIFO buffer (buffer memory) as spoken of on column 8, lines 17-20.

Regarding claim **2**, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by port vector FIFO 56 (descriptor memory) of Figure 2 that receives and decodes a forwarding descriptor corresponding to received packet data as spoken of on column 7, lines 28-34.

Lastly, "a controller coupled to the descriptor memory and the buffer memory to control data transfer between the buffer memory and the packet memory using the descriptor information" is anticipated by Internal Rules Checker (IRC) 40 (controller) of Figure 2 that uses packet header information to determine which MAC ports will output particular data frames, and then outputs a forwarding descriptor to port vector FIFO 56 (descriptor memory) that indicates a forwarding decision as spoken of on column 6, lines 58-67 as well as column 7, lines 16-27.

Regarding claims **8 and 40**, "an ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size" and a "queue

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segmenter to chunk the data stream into the at least one chunk” is anticipated by Internal rules checker 40 that snoops the data bus (data stream) to obtain frame pointer and header information of received packet data (chunk data).

Regarding claims **9 and 41**, “wherein the buffer memory comprises an input buffer memory to store the at least one chunk transferred from the queue segmenter” is anticipated by MAC unit 20 of Figure 2 that contains a transmit FIFO buffer (input buffer memory) as spoken of on column 6, lines 47-49.

Regarding claims **10 and 42**, “wherein the input buffer memory comprises a queue associated with the connection identifier, the queue having a threshold and being configured to store the at least one chunk” is anticipated by transmit FIFO buffer (queue) of MAC unit 20 of Figure 2 that receives data transferred from external memory 36 via dequeuing logic 76 of Figure 3A as spoken of on column 8, lines 20-23.

Regarding claims **11 and 43**, “wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request” is anticipated by the overflow transfer mode between queue write side 410 and overflow storage area 414 spoken of on column 11, lines 23-26.

Regarding claim **17**, “storing data associated with a connection identifier corresponding to a channel in a network in a buffer memory of a first type” is anticipated by the receive FIFO buffer (buffer memory of first type) of MAC unit 20 of Figure 2 that stores data packets having header information (connection identifier) received from network stations 14 (connection) of Figure 1 as spoken of on column 6, lines 47-61.

“The data being organized into at least one chunk based on a linked list” is anticipated by the data packets received by a corresponding MAC port and stored in a corresponding received FIFO (organized into at least one chunk).

“The connection identifier identifying a connection in the channel” is anticipated by the packet header information (connection identifier) that includes source, destination, and VLAN address information as spoken of on column 6, lines 58-61.

“The data being part of a data stream associated with the connection” is anticipated by the data packets received by MAC unit 20 of Figure 2 that are associated with a network station 14 of Figure 1.

Lastly, “providing access to the stored data using a packet memory of a second type when a transfer condition occurs, such that the data is transferred between the buffer memory and the packet memory” is anticipated by external SSRAM memory block 36 (packet memory of second type) coupled to MAC unit 20 of Figure 1 that receives burst writes of data from a corresponding receive FIFO buffer (buffer memory) as spoken of on column 8, lines 17-20.

Regarding claim 18, “storing descriptor information corresponding to the at least one chunk in a descriptor memory” is anticipated by port vector FIFO 56 (descriptor memory) of Figure 2 that receives and decodes a forwarding descriptor corresponding to received packet data as spoken of on column 7, lines 28-34.

Lastly, “controlling data transfer between the buffer memory and the packet memory using the descriptor information” is anticipated by Internal Rules Checker (IRC) 40 (controller) of Figure 2 that uses packet header information to determine which MAC

ports will output particular data frames, and then outputs a forwarding descriptor to port vector FIFO 56 (descriptor memory) that indicates a forwarding decision as spoken of on column 6, lines 58-67 as well as column 7, lines 16-27.

Regarding claim **24**, “buffering the data stream of a packet from an ingress of the channel by an ingress queue, the packet having a packet size” and “segmenting the data stream into the at least one chunk” is anticipated by Internal rules checker 40 that snoops the data bus (data stream) to obtain frame pointer and header information of received packet data (chunk data).

Regarding claim **25**, “storing the at least one chunk transferred from the queue segmenter in an input buffer memory” is anticipated by MAC unit 20 of Figure 2 that contains a transmit FIFO buffer (input buffer memory) as spoken of on column 6, lines 47-49.

Regarding claim **26**, “storing the at least one chunk in a queue associated with the connection identifier, the queue having a threshold” is anticipated by transmit FIFO buffer (queue) of MAC unit 20 of Figure 2 that receives data transferred from external memory 36 via dequeuing logic 76 of Figure 3A as spoken of on column 8, lines 20-23.

Regarding claim **27**, “wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request” is anticipated by the overflow transfer mode between queue write side 410 and overflow storage area 414 spoken of on column 11, lines 23-26.

Regarding claim **33**, “a channel in a network having an ingress and egress” is anticipated by the reduced media independent interfaces 18 (channel) of Figure 1 that



interface network stations 14 with receive FIFOs (ingress) and transmit FIFOs (egress) of MAC units 20 of Figure 1 as spoken of on column 5, lines 44-57 as well as column 6, lines 47-57.

“A data buffer circuit coupled to the channel to buffer data transmitted over the channel” is anticipated by the multiport switch 12a (data buffer circuit) of Figure 1 coupled to reduced media independent interfaces 18 (channel).

“An input buffer memory of a first type to store data associated with a connection identifier corresponding to the channel” is anticipated by the receive FIFO buffer (input buffer memory of first type) of MAC unit 20 of Figure 2 that stores data packets having header information (connection identifier) received from network stations 14 (connection) of Figure 1 as spoken of on column 6, lines 47-61.

“The data being organized into at least one chunk based on a linked list” is anticipated by the data packets received by a corresponding MAC port and stored in a corresponding received FIFO (organized into at least one chunk).

“The connection identifier identifying a connection in the channel” is anticipated by the packet header information (connection identifier) that includes source, destination, and VLAN address information as spoken of on column 6, lines 58-61.

“The data being part of a data stream associated with the connection” is anticipated by the data packets received by MAC unit 20 of Figure 2 that are associated with a network station 14 of Figure 1.

“An output buffer memory of the first type to store the data transferred from the input buffer memory” is anticipated by the transmit FIFO buffer of MAC unit 20 of Figure

2 that receives data frames retrieved from external memory 36 as spoken of on column 6, lines 47-49, as well as column 7, lines 32-39.

Lastly, “a packet memory of a second type coupled to the input and output buffer memories to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory” is anticipated by external SSRAM memory block 36 (packet memory of second type) coupled to MAC unit 20 of Figure 1 that receives burst writes of data from a corresponding receive FIFO buffer (buffer memory) as spoken of on column 8, lines 17-20.

Regarding claim **34**, “a descriptor memory to store descriptor information corresponding to the at least one chunk” is anticipated by port vector FIFO 56 (descriptor memory) of Figure 2 that receives and decodes a forwarding descriptor corresponding to received packet data as spoken of on column 7, lines 28-34.

Lastly, “a controller coupled to the descriptor memory and the input and output buffer memories to control data transfer between the buffer memories and the packet memory using the descriptor information” is anticipated by Internal Rules Checker (IRC) 40 (controller) of Figure 2 that uses packet header information to determine which MAC ports will output particular data frames, and then outputs a forwarding descriptor to port vector FIFO 56 (descriptor memory) that indicates a forwarding decision as spoken of on column 6, lines 58-67 as well as column 7, lines 16-27.

***Claim Rejections - 35 USC § 103***

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5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims **3-7, 19-23, and 35-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et al. (U.S. 6,401,147) (hereinafter "Sang") in view of Herring et al. (U.S. 6,542,502) (hereinafter "Herring").

Regarding claims **3, 19, and 35**, *Sang* teaches the apparatus of claim **2**, the method of claim **18**, and the system of claim **34**, respectively. *Sang* fails to explicitly teach storing chunk information associated with the linked list in a chunk header.

However, *Herring* teaches a next chunk field 304 (chunk header) associated with the data field of a chunk as shown in Figure 3. This field indicates the next chunk in the linked list.

At the time of the invention, it would have been obvious to someone skilled in the art to combine the chunk header field of *Herring* with the teachings of *Sang* in order to provide a way to order the packets within each packet queue as spoken of on column 3, lines 6-22 of *Herring*.

Regarding claims **4, 20, and 36**, *Sang* further teaches frame pointer entries that point to buffers in external memory (other chunk) as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **5, 21, and 37**, *Sang* further teaches frame pointer entries that point to a first buffer in external memory (head chunk) as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **6, 22, and 38**, *Sang* further teaches a forwarding descriptor (descriptor information) that contains a frame pointer (head pointer) that is used to fetch a particular data frame (head chunk) from the external memory 36 as spoken of on column 7, lines 18-39.

Regarding claims **7, 23, and 39**, *Sang* further teaches received packet header information containing source, destination, and VLAN address information corresponding to a particular frame pointer as spoken of on column 6, lines 58-64.

#### ***Allowable Subject Matter***

7. Claims **12-16, 28-32, and 44-48** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims **12-16, 28-32, and 44-48**, these claims are allowable for the reasons indicated in the previous Office Action.

#### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lyles et al. (U.S. 6,377,583) is another reference considered pertinent to this application.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:00am - 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Moore, Jr.  
Examiner  
Art Unit 2616

mjm MM

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